Microcontroller Interfacing Techniques

Document Revision: 1.01
Date: 3rd April, 2005

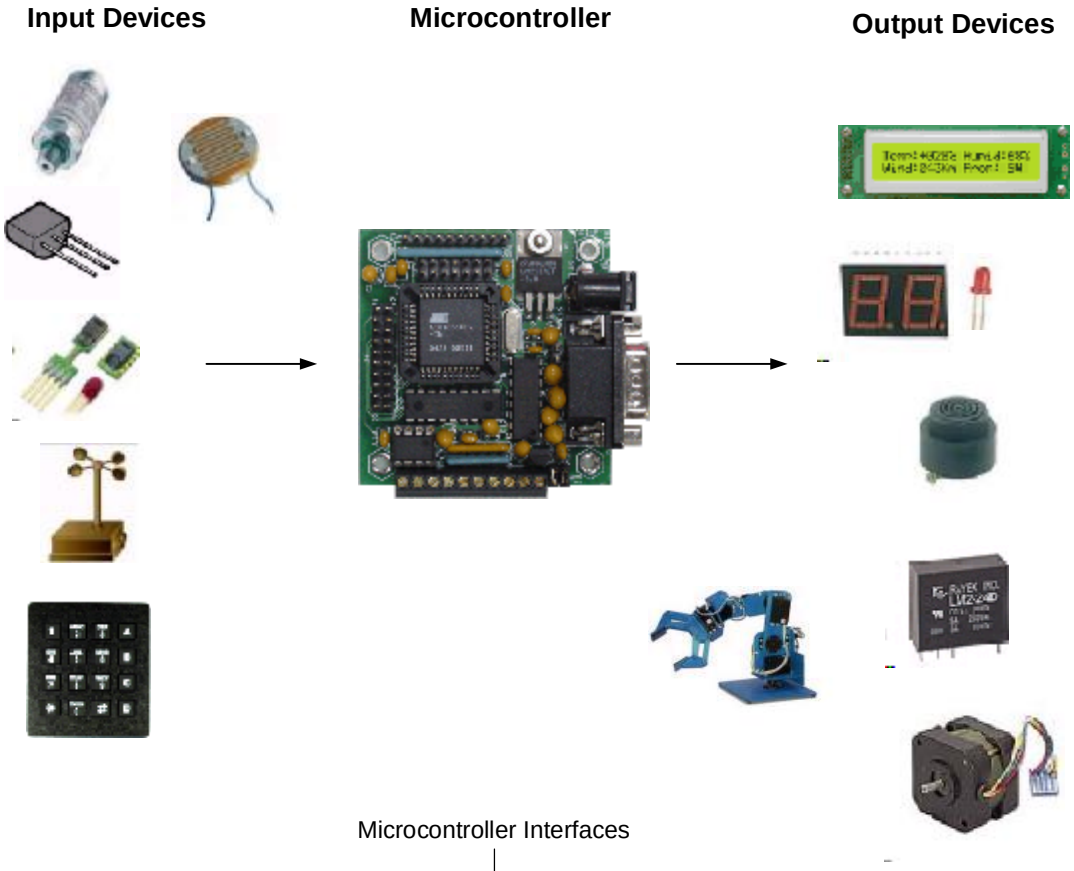
16301 Blue Ridge Road, Missouri City, Texas 77489 USA
Telephone: 1-713-283-9970 Fax: 1-281-416-2806
E-mail: info@bipom.com
Web: www.bipom.com

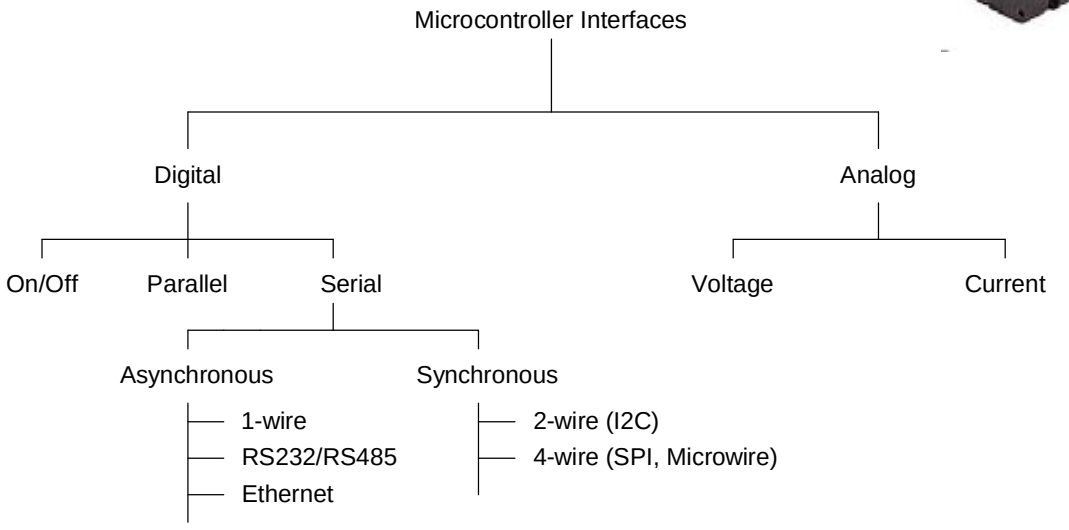
Overview

Micro-controllers are useful to the extent that they communicate with other devices, such as sensors, motors, switches, keypads, displays, memory and even other micro-controllers.

Many interface methods have been developed over the years to solve the complex problem of balancing circuit design criteria such as features, cost, size, weight, power consumption, reliability, availability, manufacturability.

Many microcontroller designs typically mix multiple interfacing methods. In a very simplistic form, a micro-controller system can be viewed as a system that reads from (monitors) inputs, performs processing and writes to (controls) outputs.





Digital Inputs/Outputs

On/OFF control and monitoring.

Advantages

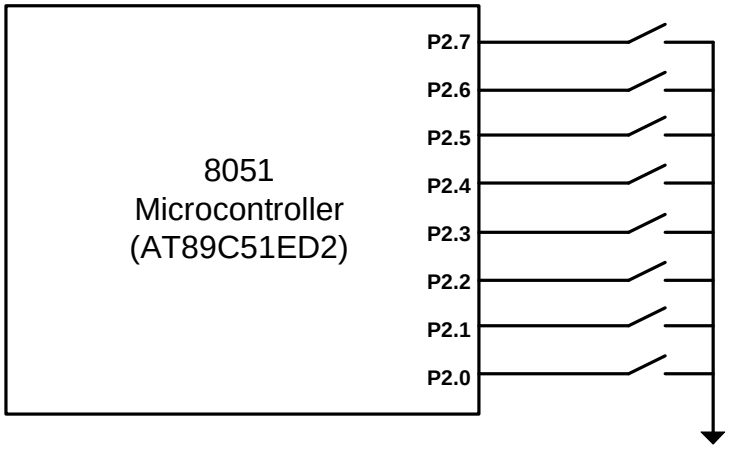
- Simplest interface
- Lowest-cost to implement (built into the microcontroller)
- High speed
- Low programming overhead

Disadvantages

- Only on/off control/monitoring
- Short distance, few feet maximum.
- Single device control/monitoring

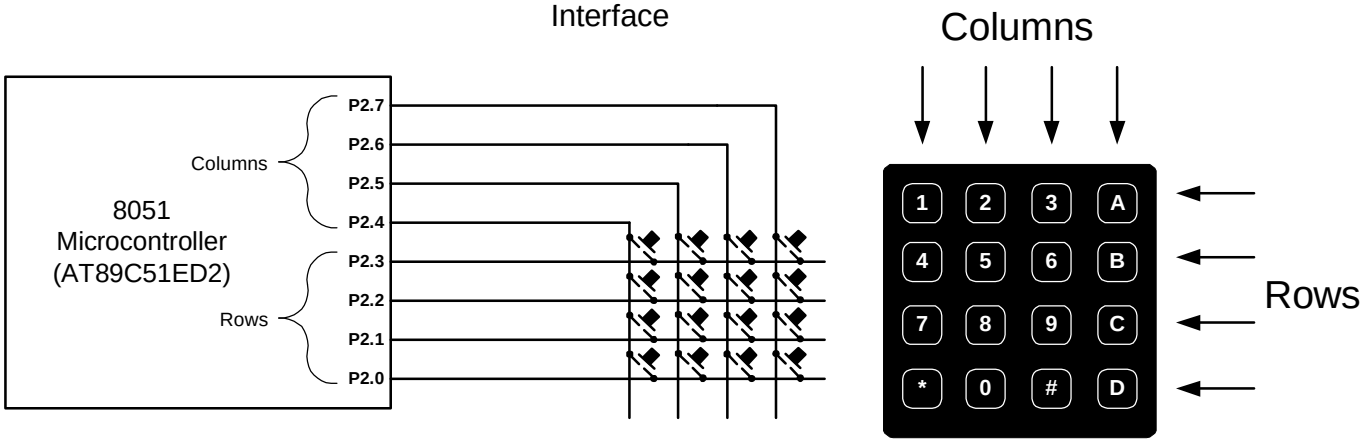
Digital Input Example: Reading the status of buttons or switches

Single-ended
(non-matrix) switches

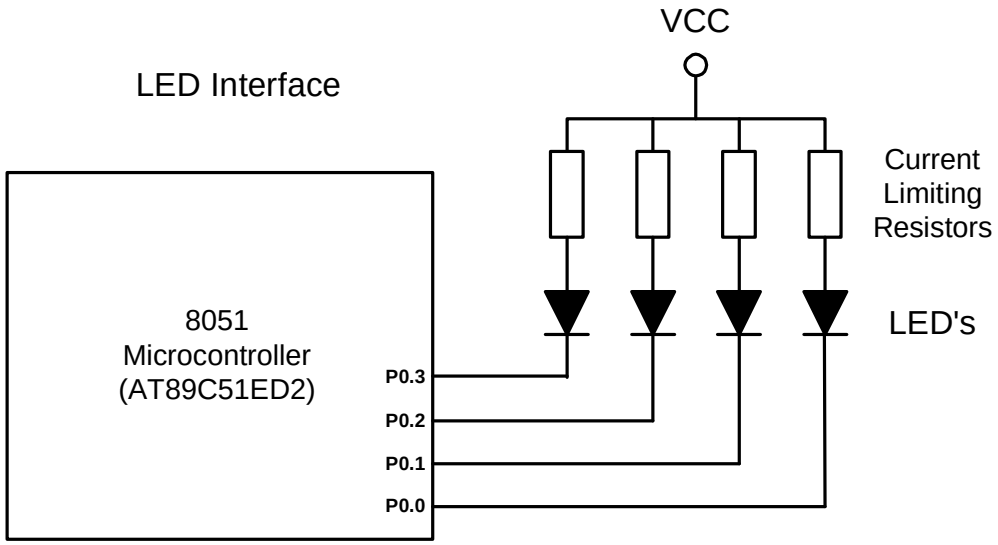


Digital Input Example: Keypad Interface

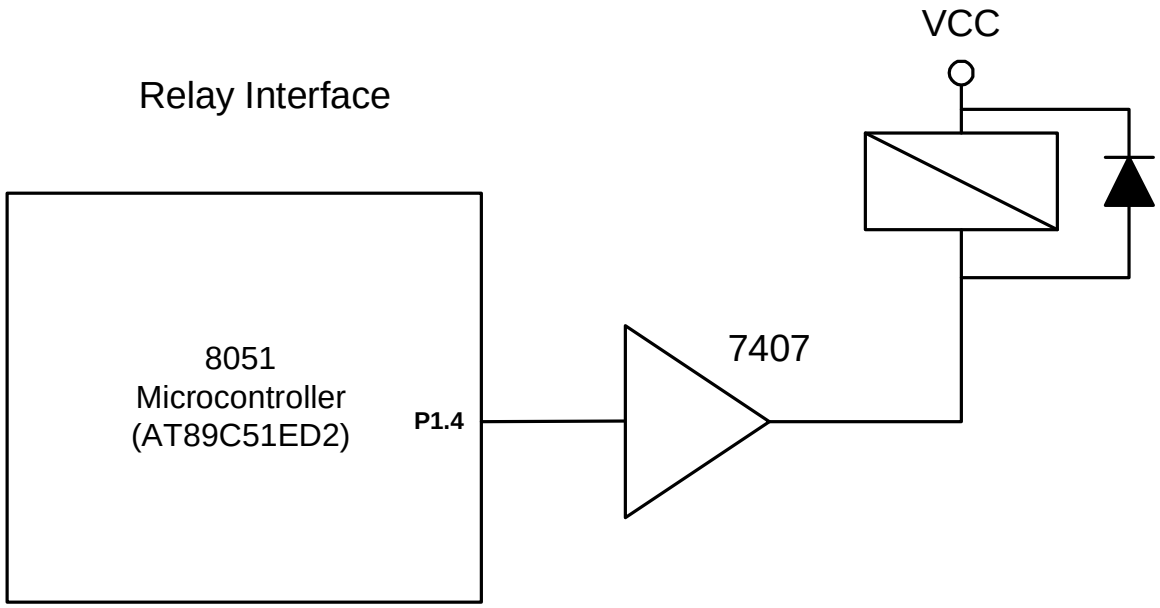
4X4 Matrix Keypad
Interface



Digital Output Example: LED control



Digital Output Example: Relay control



Analog Inputs/Outputs

Voltage-based control and monitoring.

Advantages

- Simple interface
- Low cost for low-resolutions
- High speed
- Low programming overhead

Disadvantages

- High cost for higher resolutions
- Not all microcontrollers have analog inputs/outputs built-in
- Complicates the circuit design when external ADC or DAC are needed.
- Short distance, few feet maximum.

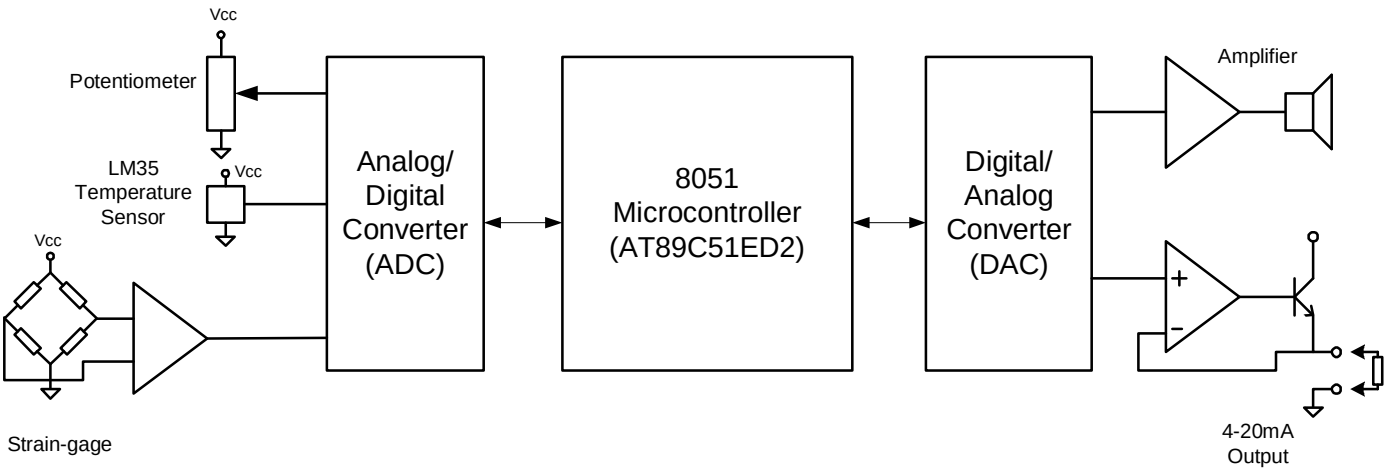
Voltage type: Typical ranges

- 0 to 2.5V
- 0 to 4V
- 0 to 5V
- +/- 2.5V
- +/- 4V
- +/- 5V

Current type: Typical ranges

- 0-20mA
- 4-20mA

Analog Interface



Parallel Bus

Consists of multiple digital inputs/outputs. Most common types:

- 4-bit
- 8-bit (e.g. Centronics)
- 16-bit (e.g. ISA)
- 32-bit (e.g. PCI)

Advantages

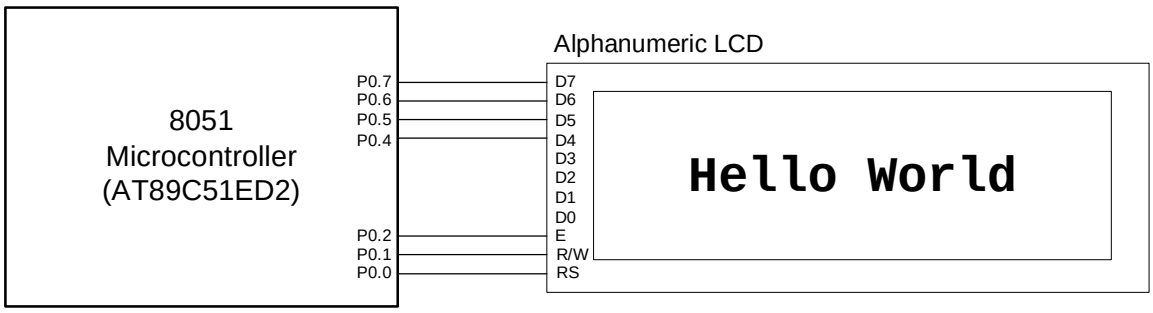
- High speed
- High throughput: Several bits are transmitted on one clock transition
- Low cost

Disadvantages

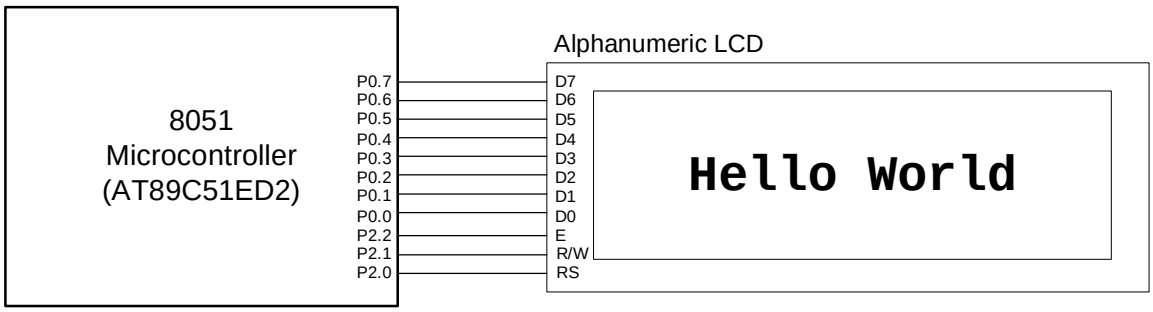
- Large number of microcontroller pins that needed for implementing the parallel bus

Example: LCD Interface

4-bit LCD Interface



8-bit LCD Interface



Serial Buses

I2C (Inter Integrated Circuit bus)

2-wire interface with one master and multiple slaves (multi-master configurations possible). Originated by Philips Semiconductor in the early 80's to connect a microcontroller to peripheral devices in TV sets.

Signals: DATA (**SDA**), CLOCK (**SCL**) and Ground. **SDA** is always bi-directional; SCL is bi-directional only in multi-master mode.

Maximum allowable capacitance on the lines is 400 pF. Typical device capacitance is 10 pF.

To start the communications, the bus master (typically a microcontroller) places the address of the device with which it intends to communicate (the slave) on the bus. All slave devices monitor the bus to determine if the master device is sending their address. Only the device with the correct address communicates with the master.

By definition, I2C is 5V.

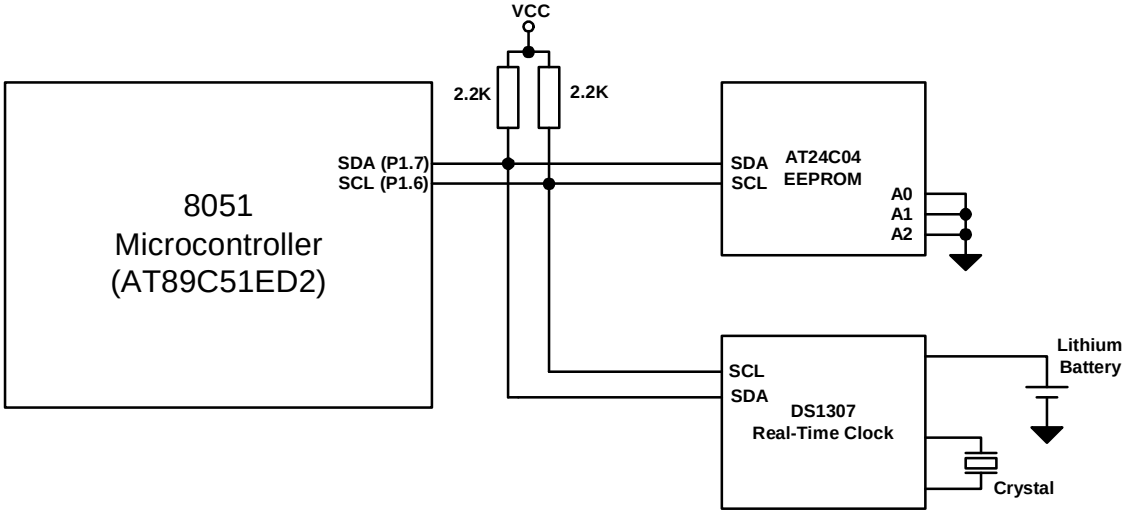
Advantages

- Multiple slave devices can be accessed with only 3 wires
- Low-cost to implement
- Implemented in hardware or software
- Ease to implement, many examples
- Supports multi-master configuration

Disadvantages

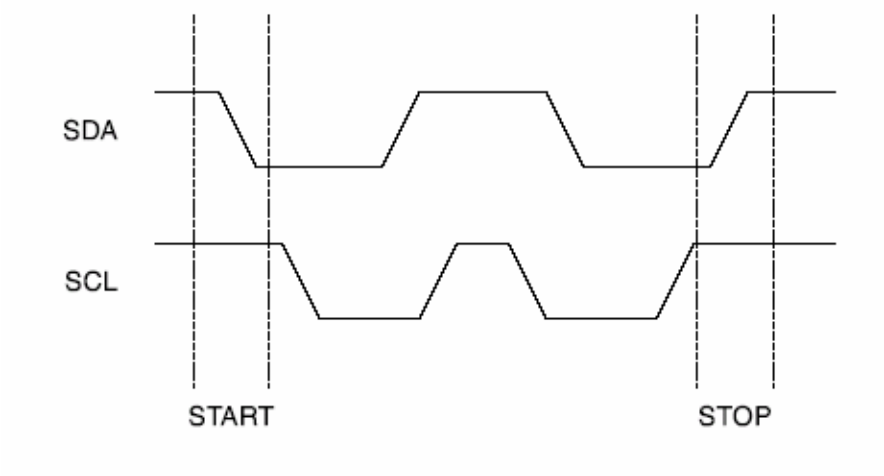
- Short distance
- Slow speed: 100 KHz although 400 KHz and 1 MHz slave devise exist. These can not coexist with slower devices.
- Limited device addresses

2-wire (I2C) interface



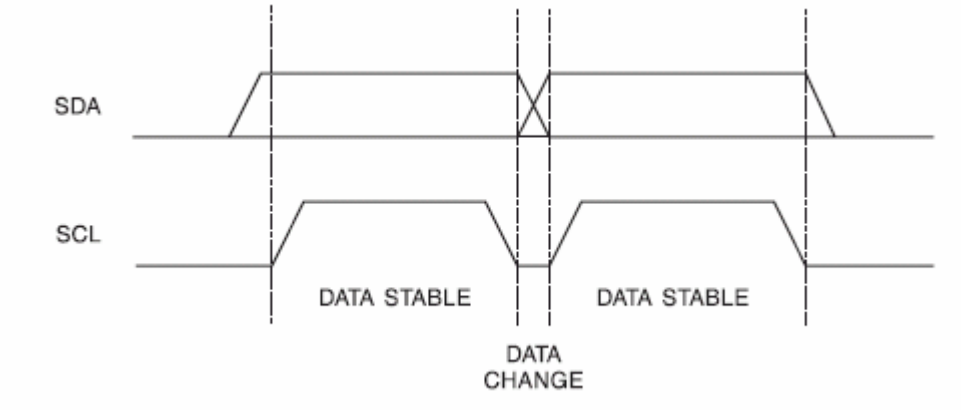
Start and Stop

An I2C master prepares to communicate with a slave device first by generating a Start condition on the bus. Start condition is defined as SDA signal going low while SCL signal is high. Stop condition is defined as SDA going high while SCL is high.

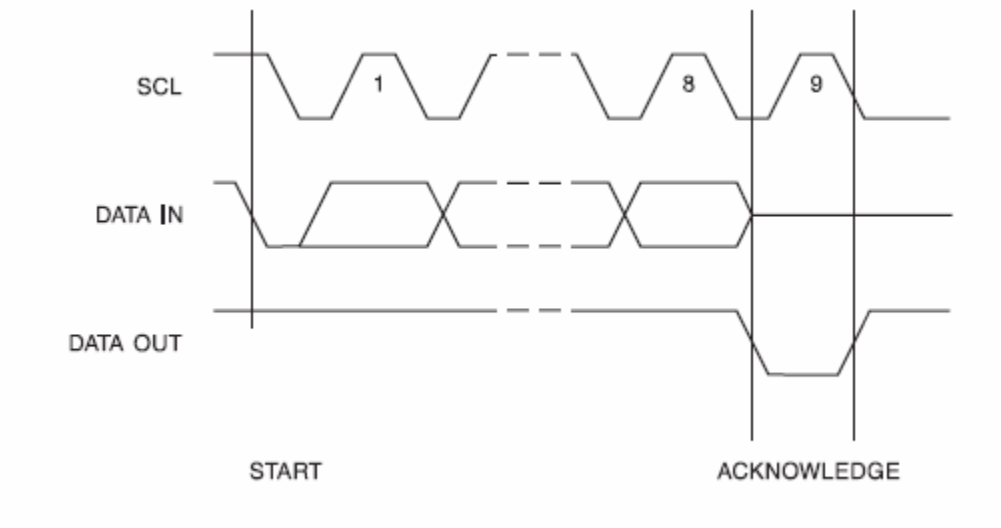


Data Validity

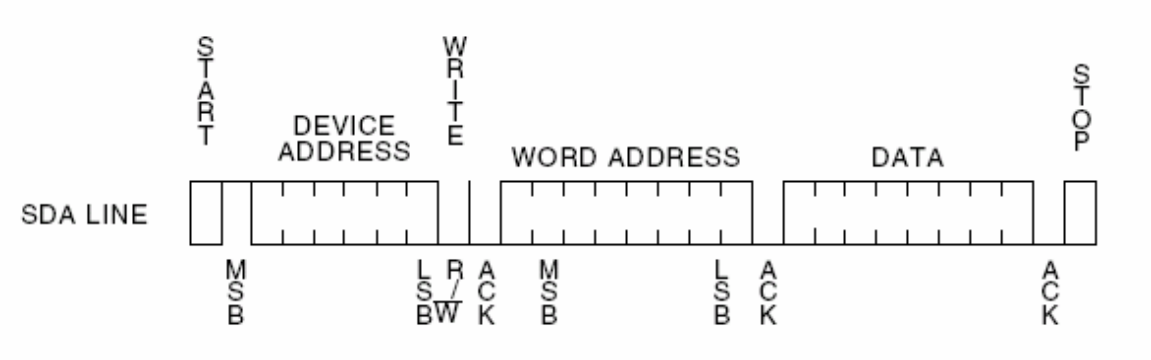
Data can change while the clock is low. Data should remain stable while the clock is going high.



Acknowledge (ACK)



Writing a byte to a serial EEPROM (24C04) on the I2C bus:



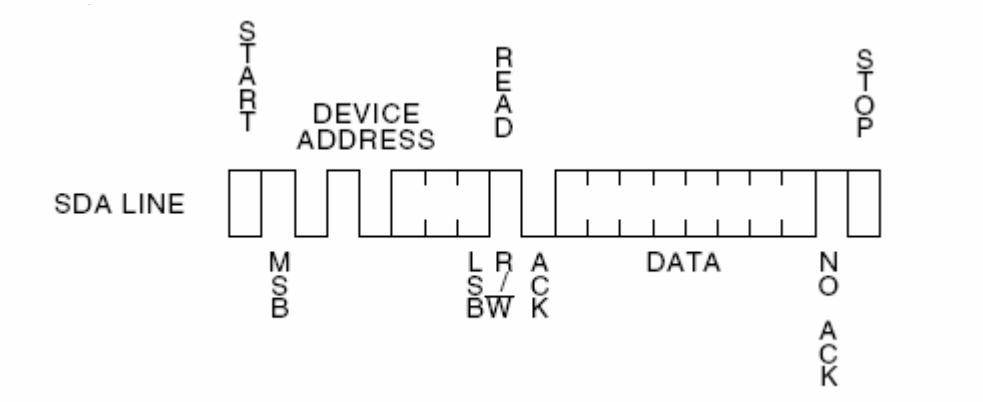
where Device Address is defined as

2K	1	0	1	0	A_2	A_1	A_0	R/W
	MSB							LSB
4K	1	0	1	0	A_2	A_1	P0	R/W
8K	1	0	1	0	A_2	P1	P0	R/W
16K	1	0	1	0	P2	P1	P0	R/W

P0, P1, P2 indicate the page number (2Kbit pages). A0, A1, A2 indicate the device number on the bus.

Reading a byte from a serial EEPROM (24C04) on the I2C bus (starting from the current address)

I



SPI (Serial Peripheral Interface)

4-wire interface with one master and multiple slaves. Signals: DATA IN, DATA OUT, CLOCK, CS (Chip Select)

Originated by Motorola, SPI bus is a relatively simple synchronous serial interface for connecting low speed external devices using minimal number of wires. A synchronous clock shifts serial data into and out of the microcontrollers in blocks of 8 bits.

SPI bus is a master/slave interface. Whenever two devices communicate, one is referred to as the "master" and the other as the "slave" device. The master drives the serial clock. SPI is full duplex: Data is simultaneously transmitted and received.

Advantages

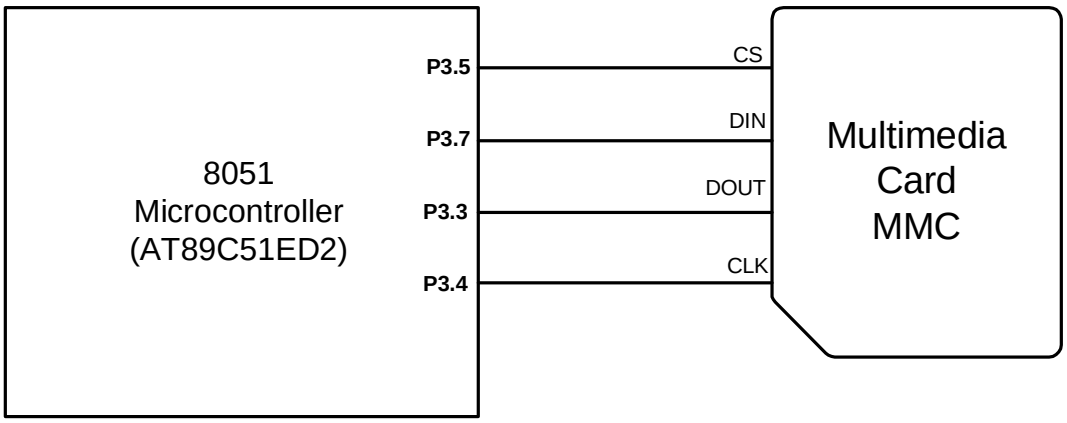
- Multiple slave devices can be accessed with only few wires
- Low-cost
- Implemented in hardware or software
- Ease to implement, many examples
- Can be high speed (e.g. 4MHz or higher if implemented in hardware)

Disadvantages

- Short distance
- Data and clock lines can be shared but each device requires a separate Chip Select signal, limiting the number of devices in limited I/O systems

Example: Multimedia Card (MMC) Interface using SPI

MMC Interface



1-wire

Originated by Dallas Semiconductor (now part of MAXIM) to address a variety of peripherals, sensors, and memory chips from a single wire interface (DATA and Ground). One signal wire carries both operating power and signal. Usually the network is built using a wire pair where one wire carries the signal and power and the other wire is ground. The system is sensitive to the right timing to operate well.

Advantages

Multiple slave devices can be accessed with only 2 wires
Low-cost
Implemented in hardware or software
Ease to implement, many examples
Relatively long distance. Theoretically 300 meters but this is limited in practice due to noise and cable capacitance

Disadvantages

- Slow speed
- 1-wire slave devices typically has to come from one source: Dallas Semiconductor

For more information on the 1-wire bus, please refer to BiPOM Application Note: Temperature Measurements with 1-Wire Bus Sensors http://www.bipom.com/applications/ds18xx_app.pdf

RS232

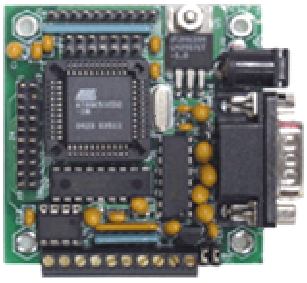
Asynchronous communications

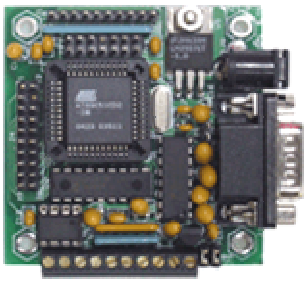
Advantages

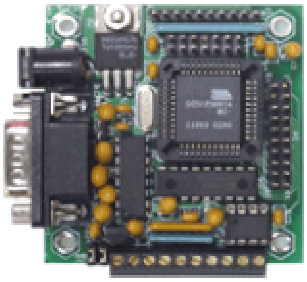
- Popular interface with many examples
- Many compatible legacy devices
- Relatively long distance, 50 feet maximum for low baud rates although longer distances work in practice, with low baud rates and error correction
- Immune to noise due to +/-5 Volts or higher voltage levels for logic “0” and “1”
- Implemented in hardware or software
- Ease to implement, many examples

Disadvantages

- More suitable for system to system communications, not so much for chip to chip or chip to sensor
- Low speed for long distance, 115200 baud can be achieved with small microcontrollers using short distances
- Requires transceiver chips which add to system cost (TTL/CMOS level RS232 can be used without transceiver chips).
- Single master/single slave





RS485

Asynchronous communications

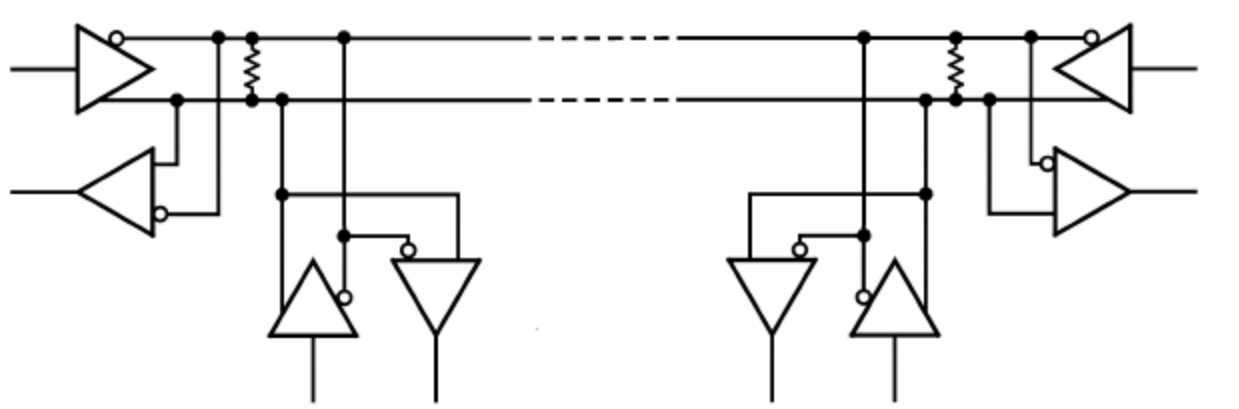
Advantages

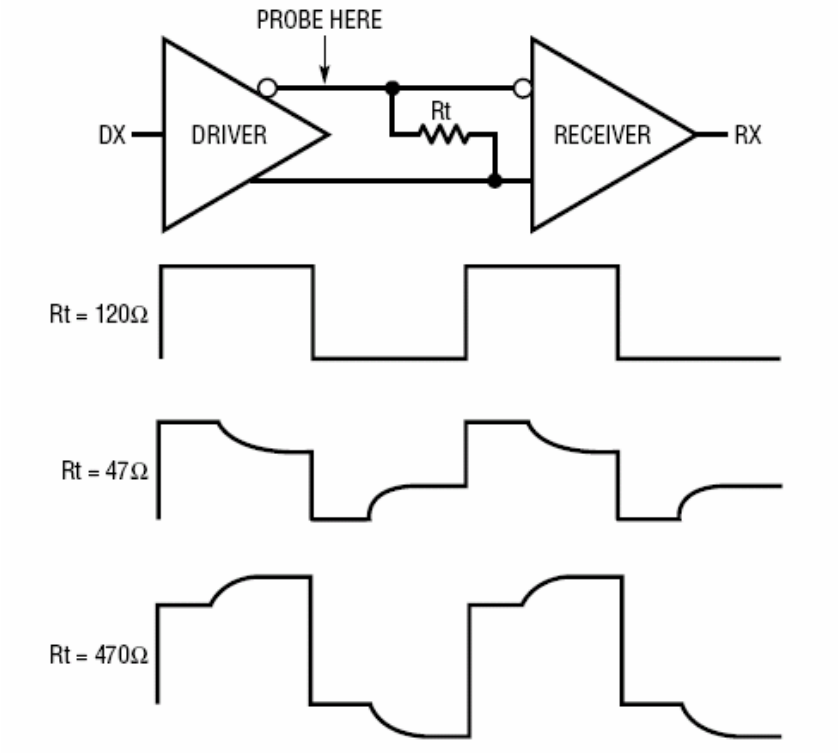
- Popular interface with many examples
- Very long distance, thousands of feet
- Immune to noise due to differential voltage
- Implemented in hardware or software
- Ease to implement, many examples
- Widely used in industrial automation
- Higher speeds beyond 115200 baud

Disadvantages

- More suitable for system to system communications, not so much for chip to chip or chip to sensor
- Requires transceiver chips and twisted pair cable with terminating resistors which add to system cost.

RS485 Network Topology: Any station can communicate with any other station, but not at the same time.





Correct termination resistor that matches the characteristic impedance of the cable is very important in RS485. Otherwise, reflected waves will result in distortions of the original waveform to the point where data errors occur.

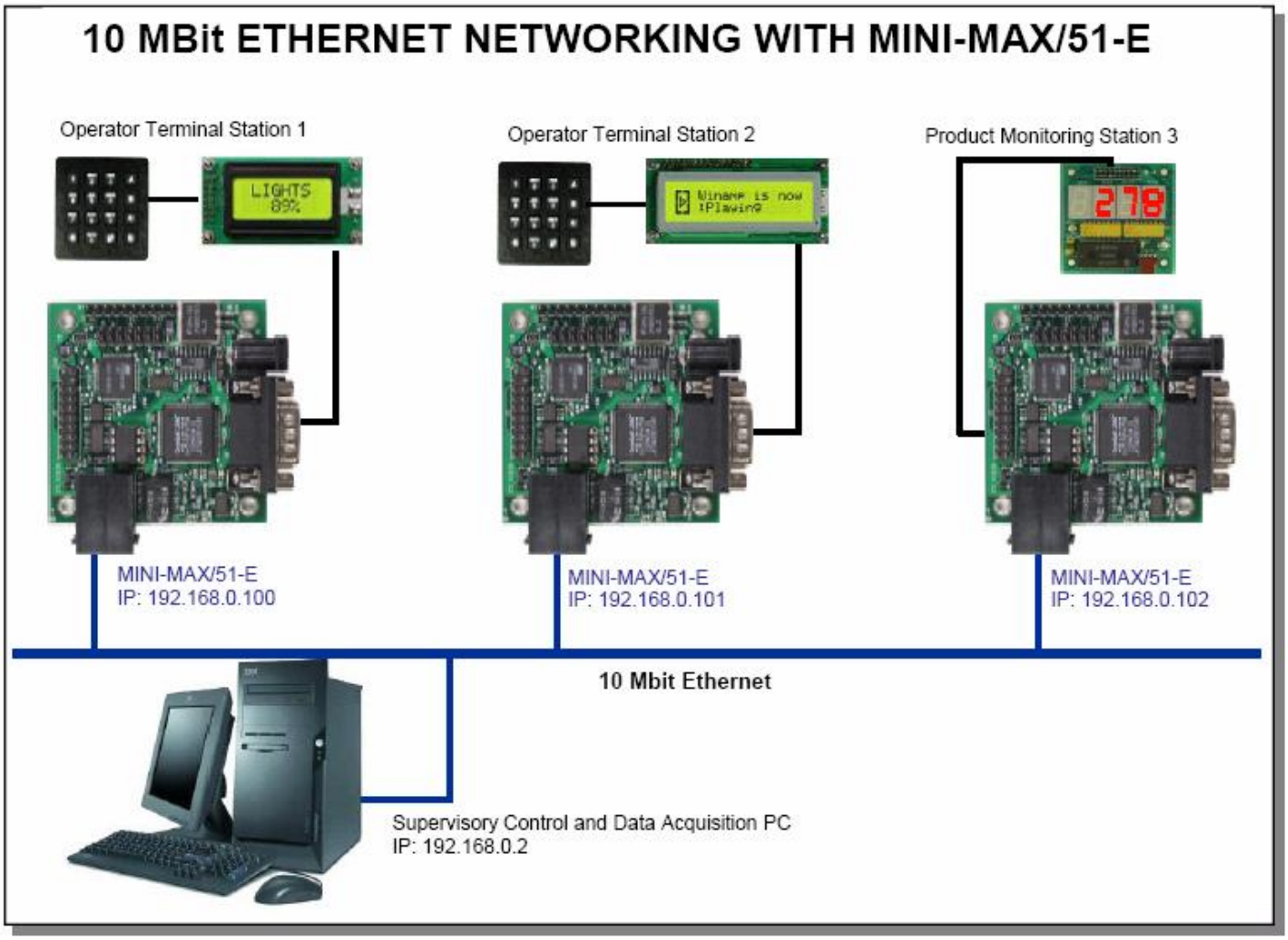
Ethernet

Advantages

- Very high speed (10Mbit to 100Mbit/s)
- Very long distance, hundreds of feet can be achieved, more with hubs and switches
- Immune to noise
- Widely used in industrial automation due to noise immunity

Disadvantages

- Cost
- More suitable for system to system communications, not so much for chip to chip/sensor
- Requires Ethernet chipset, transformer, jack and special cabling that add to system cost.
- Complicated to implement
- High code footprint



Appendix A: Comparison of Serial Digital Data Networks (from MAXIM website: www.maxim-ic.com)

	1-Wire	I^2C*	SMBUS™	SPI™	MicroWire/PLUS™	M-Bus (EN1434)	CAN (ISO11898)	LIN Bus
Network Concept	single master, multiple slaves	multiple masters, multiple slaves	multiple masters, multiple slaves	single master, multiple slaves	single master, multiple slaves	single master, multiple slaves	multiple masters, multiple slaves	single master, multiple slaves
Number of Signal Lines	1 (IO)	2, (SCL, SDA)	2, (SMBCLK, SMBDAT)	4, (CS\, SI, SO, SCK)	4, (CS\, DI, DO, SK)	2 (lines can be swapped)	2 (CAN_H, CAN_L, terminated)	1 (LIN)
Optional signals	N/A	N/A	SMBSUS#, SMBALERT#	N/A	N/A	N/A	2nd GND, Power, Shield	N/A
Network Size	Up to 300 m (with suitable master circuit)	Limited by max. 400pF bus capacitance requirement	Limited by max. 400pF bus capacitance requirement	N/A (circuit board level)	N/A (circuit board level)	Max. 350m per segment of max. 250 slaves; max. 180nF	40m @1M bps1000m @ 50k bps (example)	Up to 40m, max. 10nF total load
Network Interface	open drain, resistive or active master pull-up	open drain, resistive or active master pull-up	open drain, resistive or active master pull-up	Push-pull with tristate	Push-pull with tristate	M to S: voltage drive S to M: current load	Differential open drain/source or open coll./emitter	open drain, resistive master pull-up
Network Voltage	From 2.8 to 6.0 V, device specific	From 1.8 to 5.5V, device specific	2.7V to 5.5V	From 1.8V to 5.5V, device specific	From 1.8V to 5.5V, device specific	~40V	V_{DD}-VD (diode drop); ~4.5V max.	8 to 18V
Logic Thresholds	Vary with network voltage	Fixed level: >1.5V, >3.0 V V_{DD}-related level: <30%, >70% of V_{DD}	<0.8V, >2.1V	V_{DD}-related level: <20% (30%), >70% of V_{DD} (inconsistent)	Fixed level: <0.8V, >2.0V; V_{DD}-related level: <20% (30%), >70% (80%) of V_{DD} (inconsistent)	Master to slave: 24V, 36V nominalSlave to master: <1.5mA, >11mA	Differential: <50mV (recessive), >1.5V (dominant); driver specification	V_{DD}-related level: <20%, >80% of V_{DD} (driver spec.)<40%, >60% of V_{DD} (receiver spec.)
Transmission	LS bit first, half-duplex	MS bit first plus Acknowledge bit, half-duplex	MS bit first plus Acknowledge bit, half-duplex	MS bit first, full-duplex	MS bit first, full-duplex	LS bit first, half-duplex, acknowledge response	MS bit first, half-duplex	LS bit first, half-duplex
Address Format	56 bits	7 bits, (10 bits defined but not implemented)	7 bits, (10 bits defined but not implemented)	N/A	N/A	8 bits (primary address), 64 bits (secondary address)	Message identifier 11 bits (standard format), 29 bits (extended format)	Message identifier 8 bits, including 2 parity bits
Network Inventory	Automatic, supports dynamic topology change	N/A; slave addresses hard-coded in firmware	ARP, Address Resolution Protocol (Rev. 2.0 only)	N/A; slave select (CS\) hard-coded in firmware	N/A; slave select (CS\) hard-coded in firmware	Automatic	N/A; message-based protocol, not address based	N/A; message-based protocol, not address based
Gross Data Rate	Standard: ~0 to 16.3k bps Overdrive: ~0 to 142k bps)	Standard: ~0 to 100k bps; Fast: ~0 to 400k bps; High-Speed: ~0 to 3.4M bps	10k to 100k bps	~0 to ~10 M bps (device specific)	~0 to ~5 M bps (device specific)	300, 2400, 9600 bps	~0 to 1M bps	~1k to ~20k bps
Access Time	Standard: ~ 5.4ms Overdrive: ~0.6ms (at maximum speed)	Standard: ~95µsFast: ~23µs(at maximum speed)	~95µs @ 100k bps	N/A	N/A	Primary address, 2400 bps: 13.75ms (short frame), 27.5ms (long frame)	At 1M bps 19µs (standard) or 39µs (extended) from start of frame to 1st data bit	At 20k bps 1.7ms from start of frame to 1st data bit
Data Protection	8-bit and 16-bit CRC	N/A	PEC Packet Error Code (Rev.1.1, 2.0)	N/A	N/A	Even parity, check sum, frames	15-bit CRC, frames, frame acknowledge	Check sum, frames
Collision Detection	Yes, through non-matching CRC	Yes (multi-master operation only)	Yes (Rev. 2.0 only)	N/A	N/A	Yes ("medium" and "strong" collisions)	Yes: CSMA/CD	Yes, through check sum
Slave supply	Parasitic (typical), V_{DD} (exception)	V_{DD} only	V_{DD} only	V_{DD} only	V_{DD} only	Parasitic and/or local supply	V_{DD} only, local or remote source	Parasitic only